

Modelization and simulation of intermittent stuck bits phenomenon

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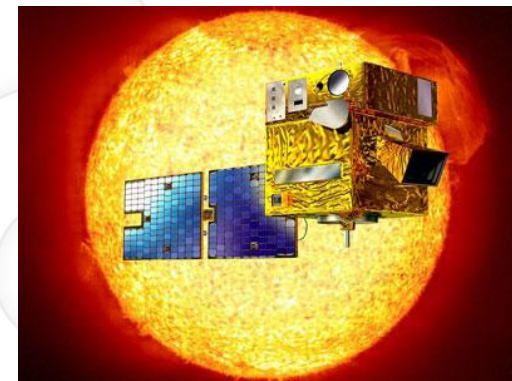
IES, Montpellier 12/02/2018

Briefly about the subject

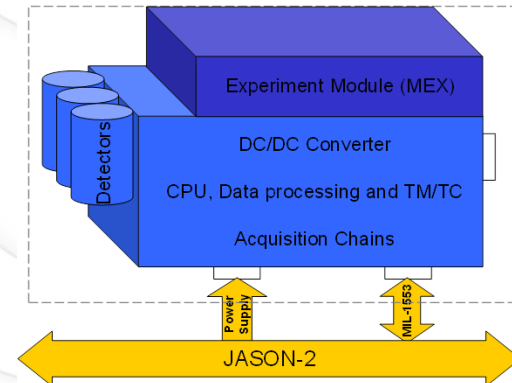
Errors appears on board CNES satellite : memory of Star Tracker on PICARD and CARMEN2/JASON2
(A.Samaras "Experimental characterization and In-flight observation of Weakened cell in SDRAM")

Previous studies by Axel Rodrigues:
Reproduce these errors at ground level
Characterize the behavior of faulty SDRAM cells
Study the mechanism and origin of phenomenon
Simulation with TCAD software (ecorce)

My work:
Modelization and simulation of the phenomenon



CARMEN-2 aboard JASON-2



SDRAM technology

SDRAM - Synchronous Dynamic Random Access Memory

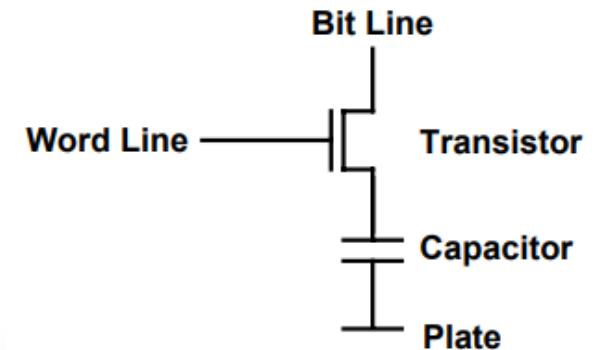
Characteristics:

Volatile

SDRAM cell is made up of a single MOS transistor and a storage capacitor

Need refresh to keep charges

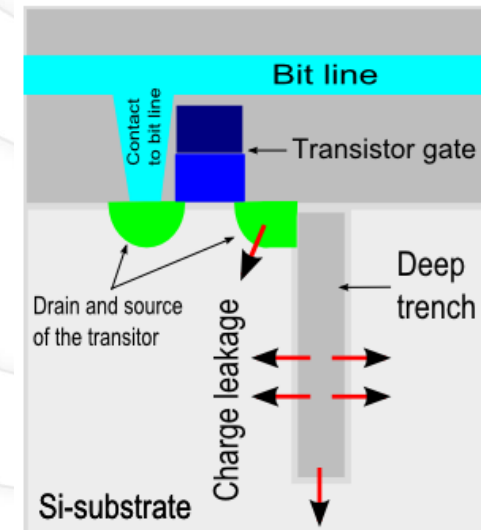
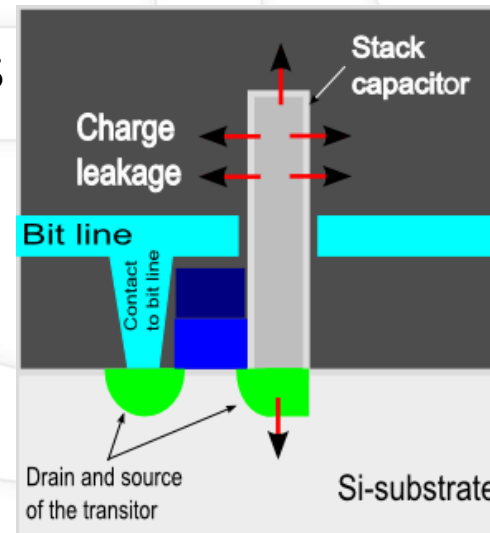
Susceptible with radiation effects



Source: ICE, "Memory 1997"

19941

1T/1C DRAM cell

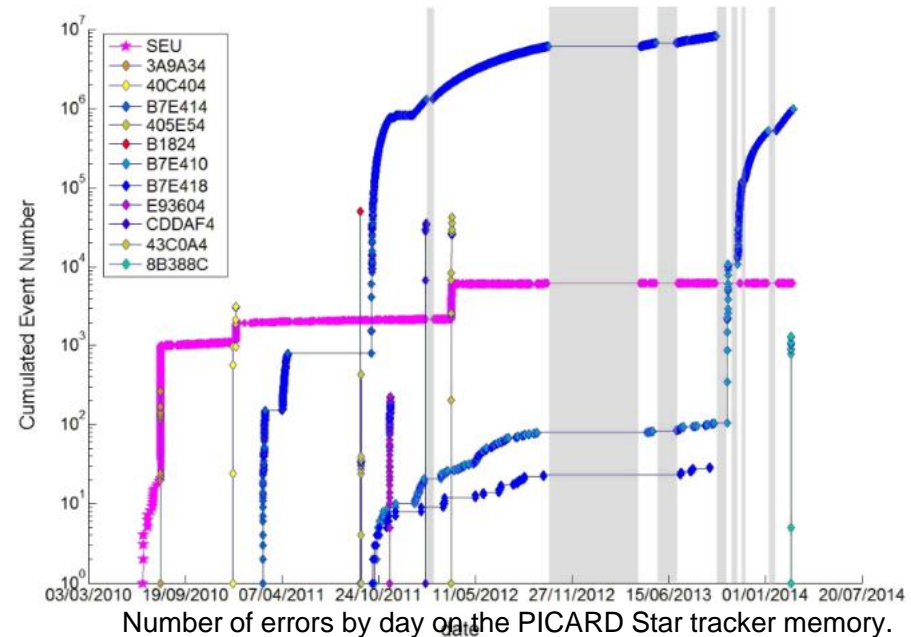


(Credit: sdram-technology)

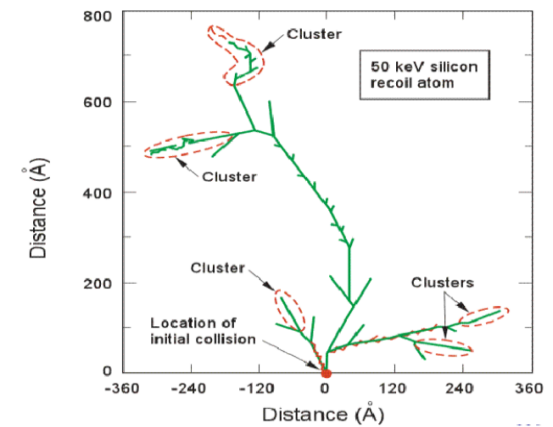
Intermittent Stuck Bits - ISBs

- Observation repeated errors in memory of PICARD Star tracker and in CARMEN2 experiment.
- Characteristics:
Localized : happen on preferential address
Intermittent : the errors disappear after a period of time
Persistent : restart devices do not fix the error
⇒ Not SEU or Stuck bits
- Strongly because:
Displacement damage cluster inside the depletion region

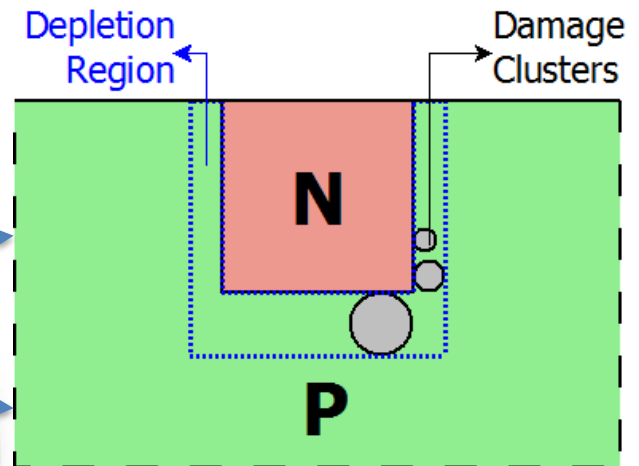
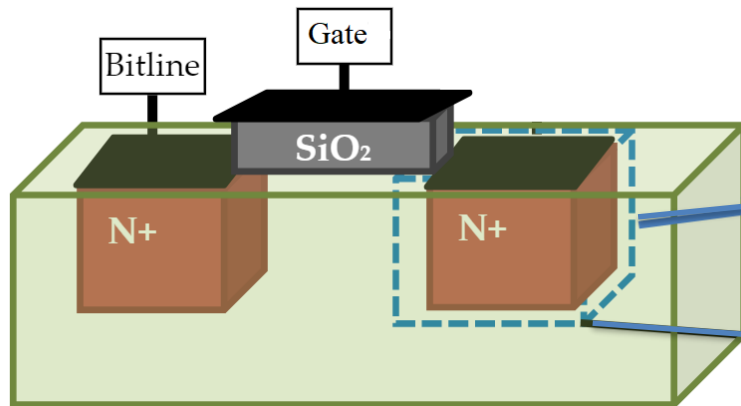
[L. D. Edmonds and L. Z. Scheick "Physical Mechanisms of Ion-Induced Stuck Bits in the Hyundai 16M 4 SDRAM "]



Number of errors by day on the PICARD Star tracker memory.
The pink color is the total number of non-recurring errors

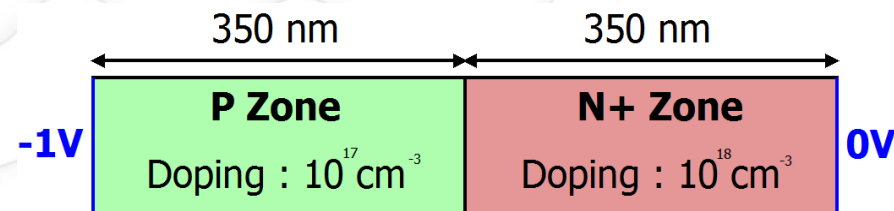


PN Junction simulation

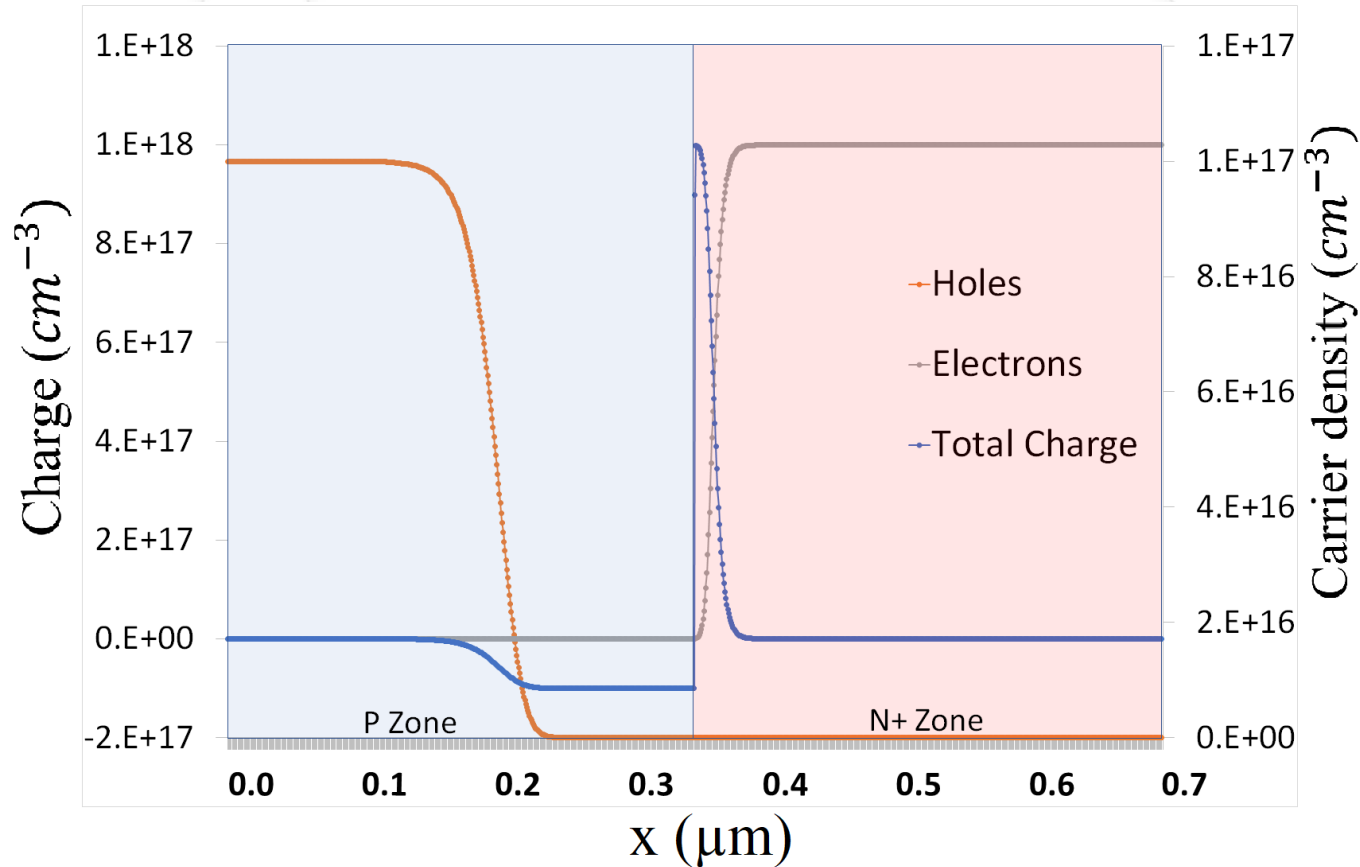


Junction dimensions	700 nm
P zone dimension	350 nm
P zone doping (cm^{-3})	1×10^{17}
P zone contact bias (V)	-1
N+ zone dimension	350 nm
N+ zone doping (cm^{-3})	1×10^{18}
N+ zone contact bias (V)	0

Size of cluster	20-100nm
Trap density cm^{-3}	$1 \times 10^{18} - 1 \times 10^{20}$
Type	Acceptor
Trap energy	0.56 eV

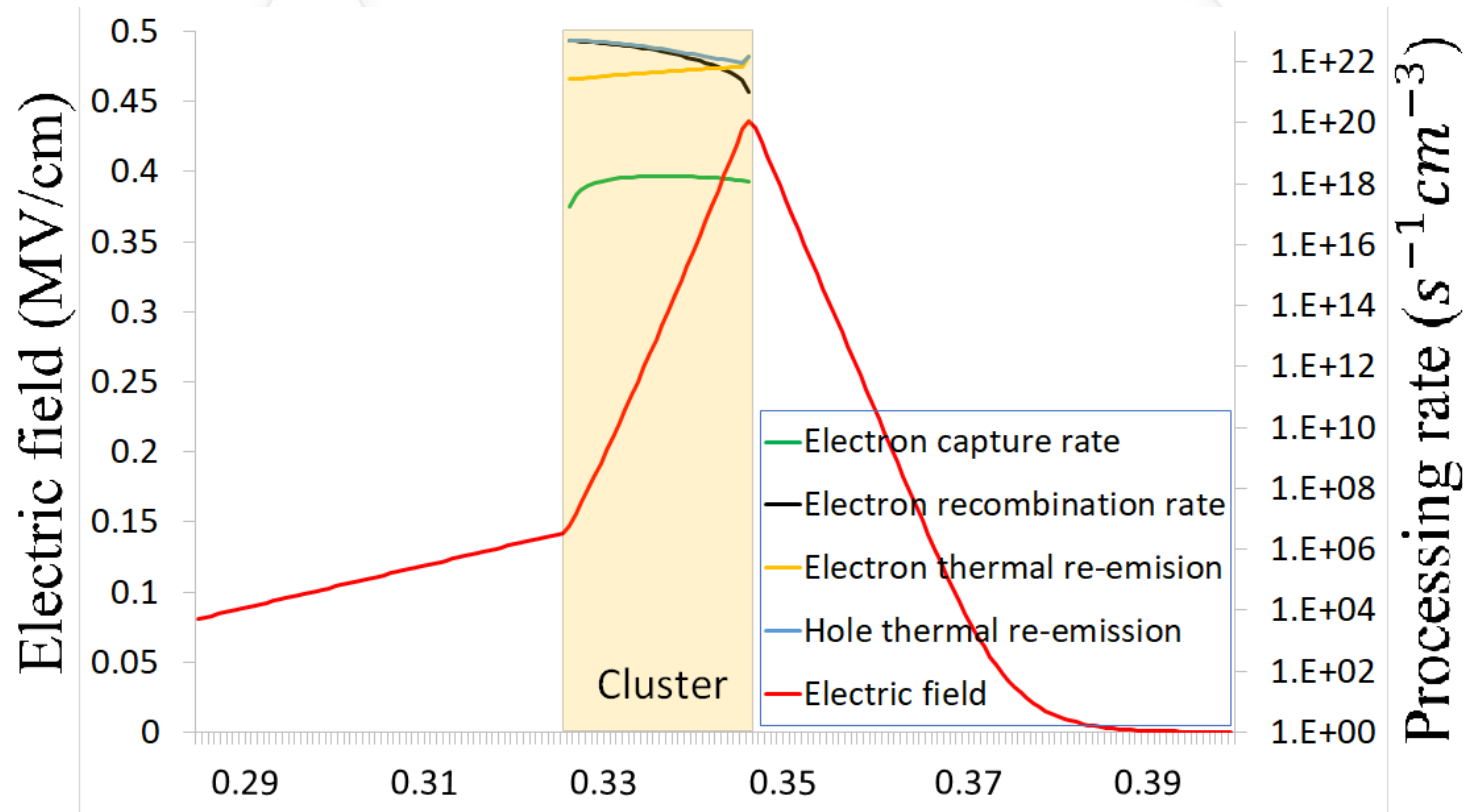


Pristine device



Consider discharge as RC circuit
Capacitance of 20fF – 40 fF : 1700 s retention time

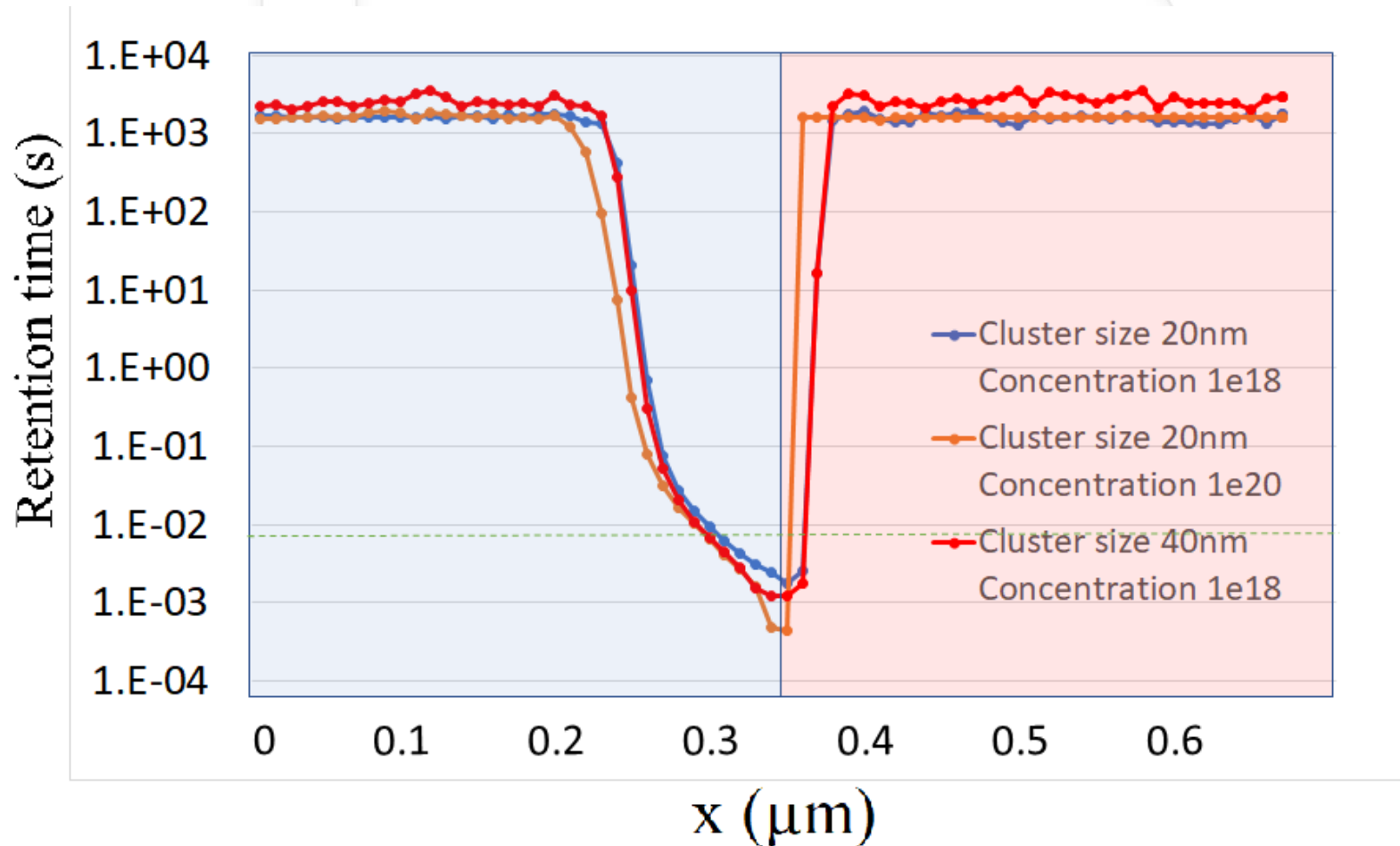
Basic mechanisms occurred



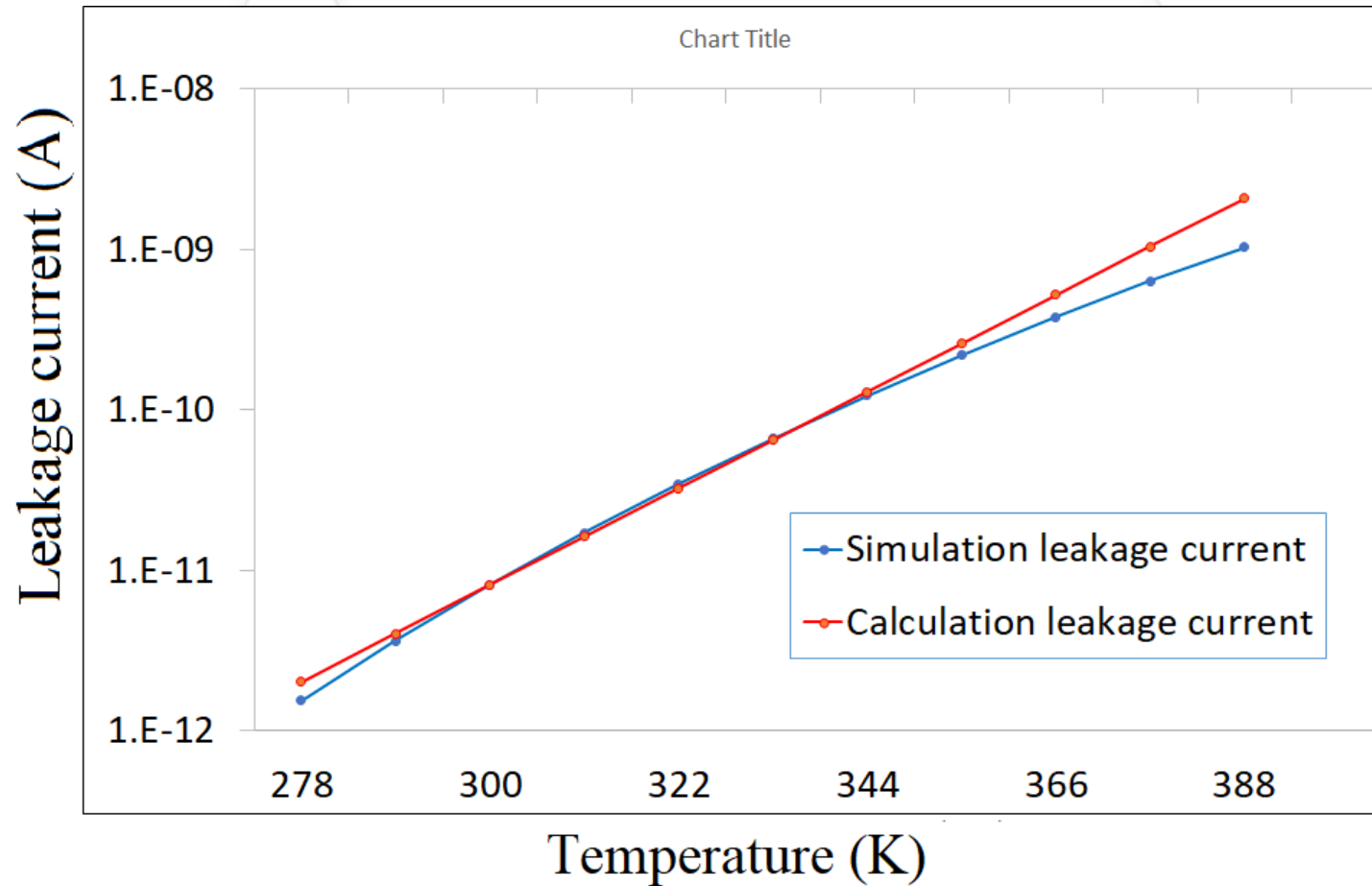
Carriers are generated by the following process :
 Acceptor states thermally emit holes, creating trapped electrons.
 A part of generated holes recombine with the trapped electrons.
 The most part of remaining electrons is thermally reemitted

Simulation Result

Cluster position and retention time with different size and density of cluster



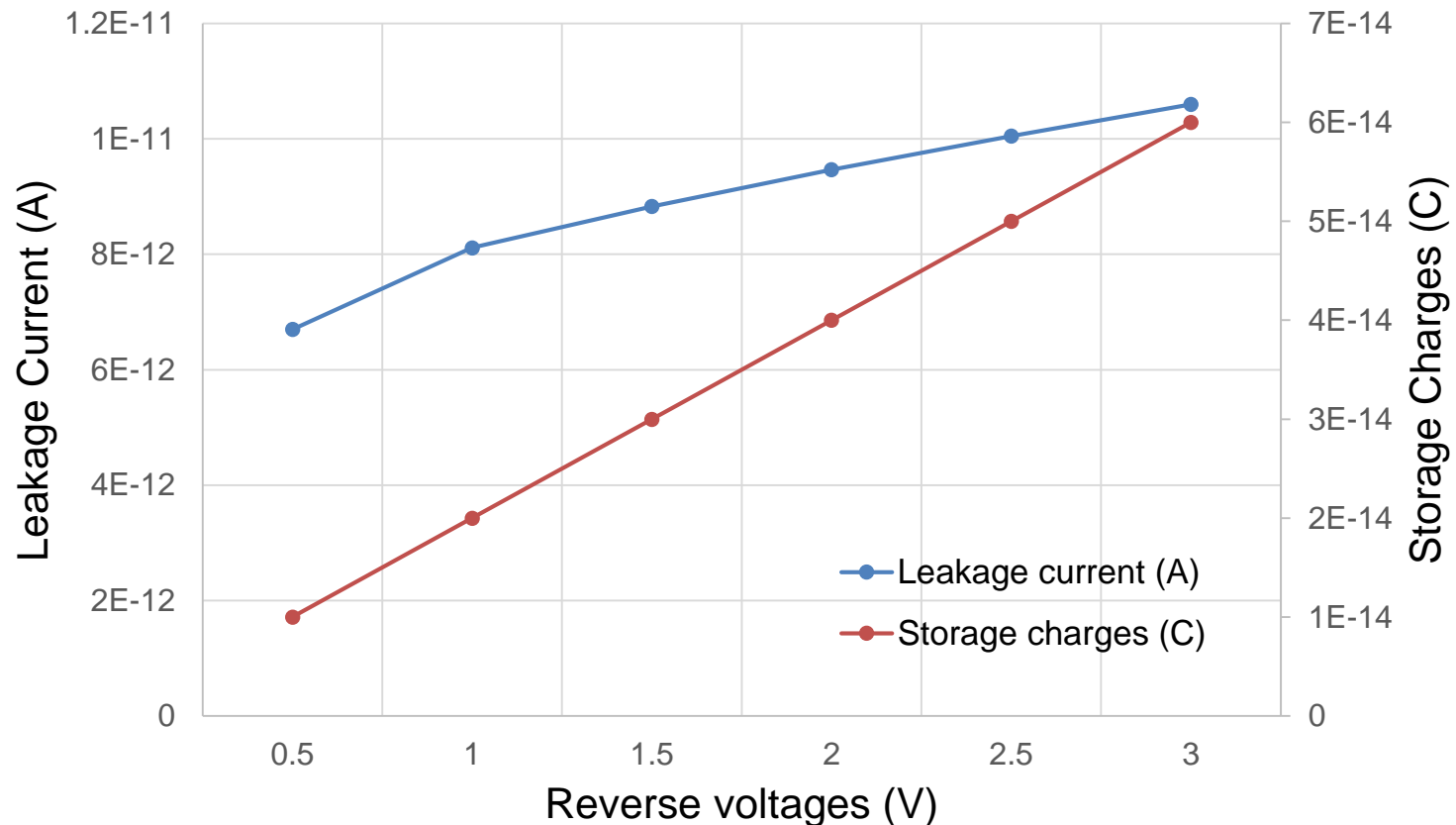
Temperature effect



Leakage current is double every 11 K

[Philippe C. Adell et.al "An Approach to Single Event Testing of SDRAMs "]

Voltage applied effect



Lowering storage node voltage will increase the drop of retention time.
Increasing storage node voltage, decreases the drop of retention time created.

What's next ?

- Simulation on the total DRAM cell including capacitor; in 2D with cluster implementation
- Study the phenomenon on different trapping/detrapping energy level (previous at 0.56ev), and on different temperature.
- Building different models of displacement damage cluster (previous Gossick model) with time dependence configuration.
- Experiment with devices under beam for functional test, retention time measurement. Examination annealing effect and temperature effect.



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Thank you for listening !

Back up - memory Technology

Non volatile

EEPROM
Flash
Other

Persistent values, Great capacity, lower
power consumption
Slower access times, throughput

Apps: start-up memory, persistent storage

Volatile

SRAM
DRAM

Values are not persistent, Lower capacity
Increased power dissipation
Fast access times, throughput

Apps: run-time memory, buffering

Variations of the 6T cross-coupled inverters
with buffers
Self-reinforcing nature improves SEE
performance
SEFI modes not as varied and often not as
complex