Modeling cumulative dose effects (TID) on UDSM technology on SOI

CNES supervisor :
Florance Malou

IES supervisors :
Frédéric Saigné,
Alain Michez

MICROCHIP supervisors :
Eric Leduc,
Severine Furic

PhD student : Flavien Perez

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Objective & Background

Context and objectives

- Radiation in space
  - Cosmic ray
  - Solar wind
  - Radiation belt
- Two principles effects on device
  - Single event
  - Dose

Objective & Background

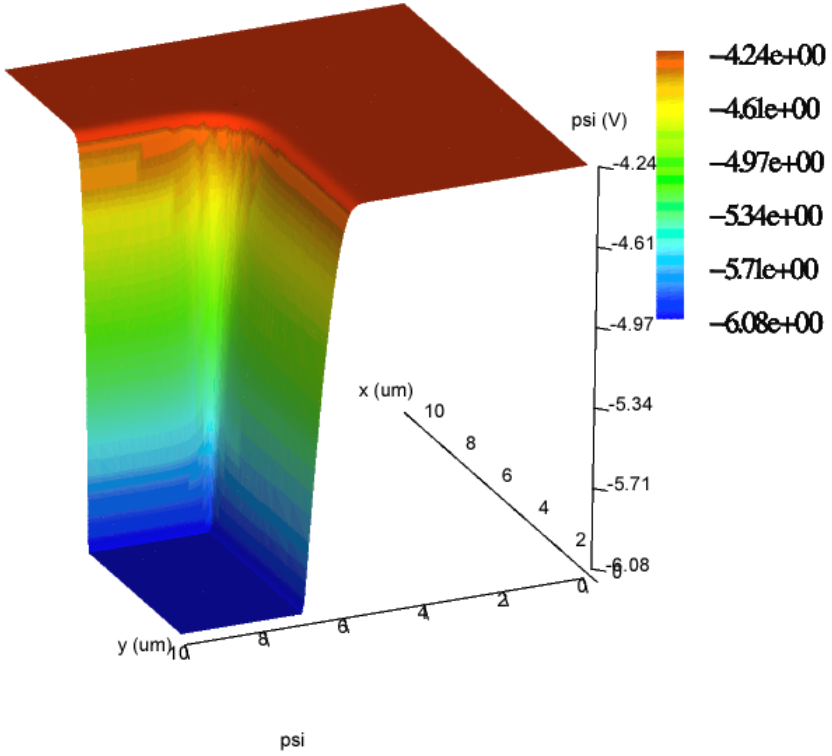
Purpose of my Phd :

To study the effects of the Total dose effect (TID) on Global Foundry FDSOI22 nm technology for a further application in space by using predictive TCAD simulation and experiment, co-funded by CNES and Microchip

TCAD tool

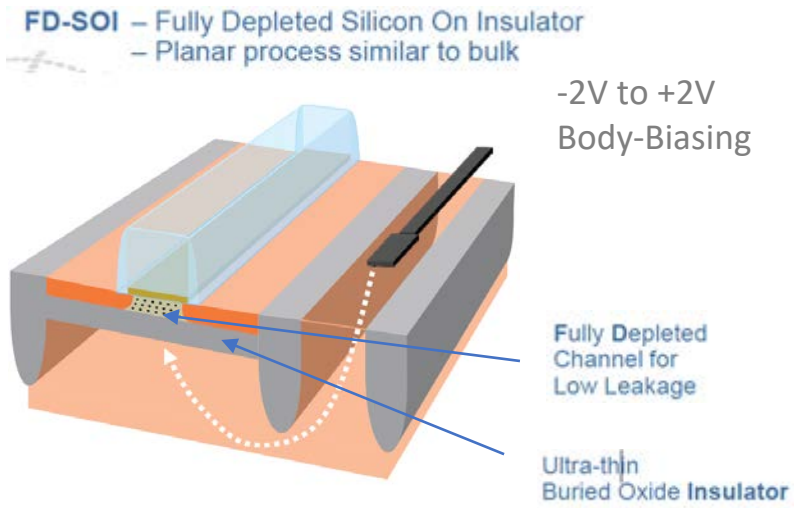
ECORCE

- TCAD simulation tool
  - Developed in the Radiac team at IES by Alain Michez
- 1D or 2D simulation
- ECORCE use a dynamic mesh to simulate the transport of carrier



PhD project

1. First use ECORCE on known PDSOI150 nm technology from Microchip
   1. Methodology
      1. Compare electrical simulation between spice and ECORCE on the 150 nm technlogy
      2. Compare dose experiment data and dose simulation with ECORCE
         - Goal : Validate the coherence of ECORCE on a well-known technology
2. ECORCE TCAD Tool for theoretical TID study on FDSOI technology
   1. State of the art of FDSOI technoloy and TID effects on FDSOI technologies
   2. Use the same methodology than the PDSOI150 nm
      1. Electrical characterization of elementary devices of FDSOI22nm GF
      2. TID simulation on the FDSOI22nm GF
3. Start experiment on FDSOI22 nm GF
   1. TID experiment with cobalt-60 source and X-rays
   2. Extraction of energy level of oxide traps participating to cumulated dose



FDSOI22 nm of Global Foundry
(Artist view)

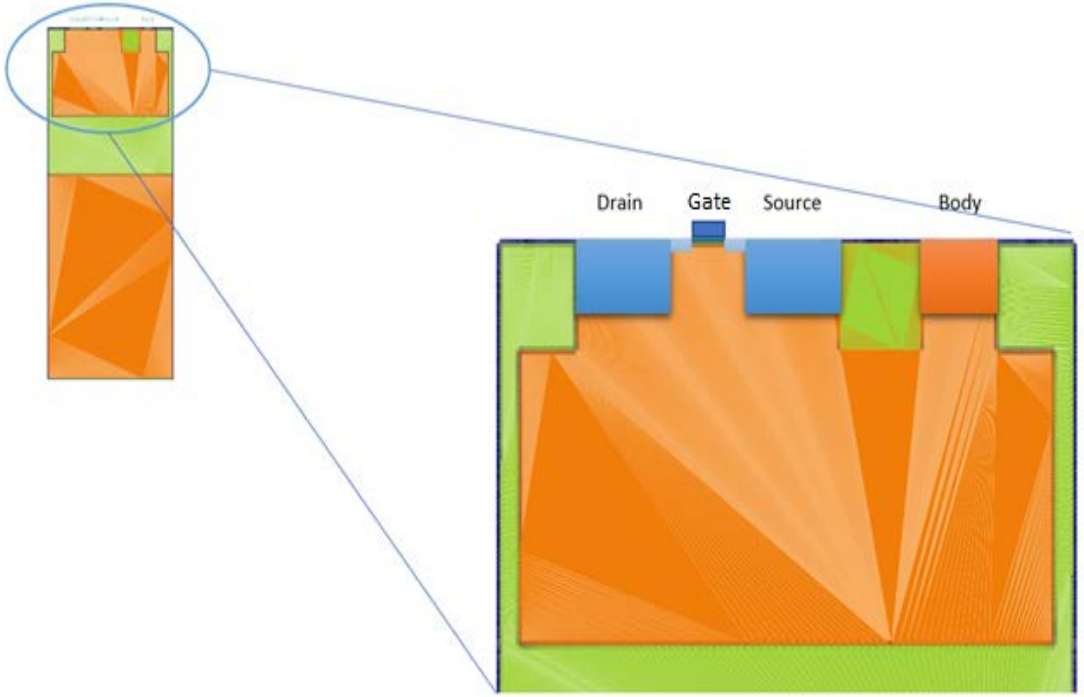
PhD project

4. Road to the UDSM technology

1. TID hardening strategy for FDSOI technologies
2. TID hardening strategy proposals for UDSM technologies from 22nm to 12nm
3. Hardening solutions through proposals of PCM structures

Study of the Atmel/MCP PDSOI150 nm technology

- Study of the behavior of MOS at the dose
  - NMOS 1,8V, 3.3V & 5V
  - PMOS 1,8V, 3.3V & 5V
- Modelization par ECORCE
  - Geometrical model
  - Doping profile
    - Approximative doping profile for the moment
- Simulation of the electrical behavior of transistors
  - ECORCE simulation
  - Comparisons with simulations Spice before radiation and before integration of the real doping profile
- Simulation of the dose effect on components
  - ECORCE simulation
  - Comparison with experimental measurements after TID

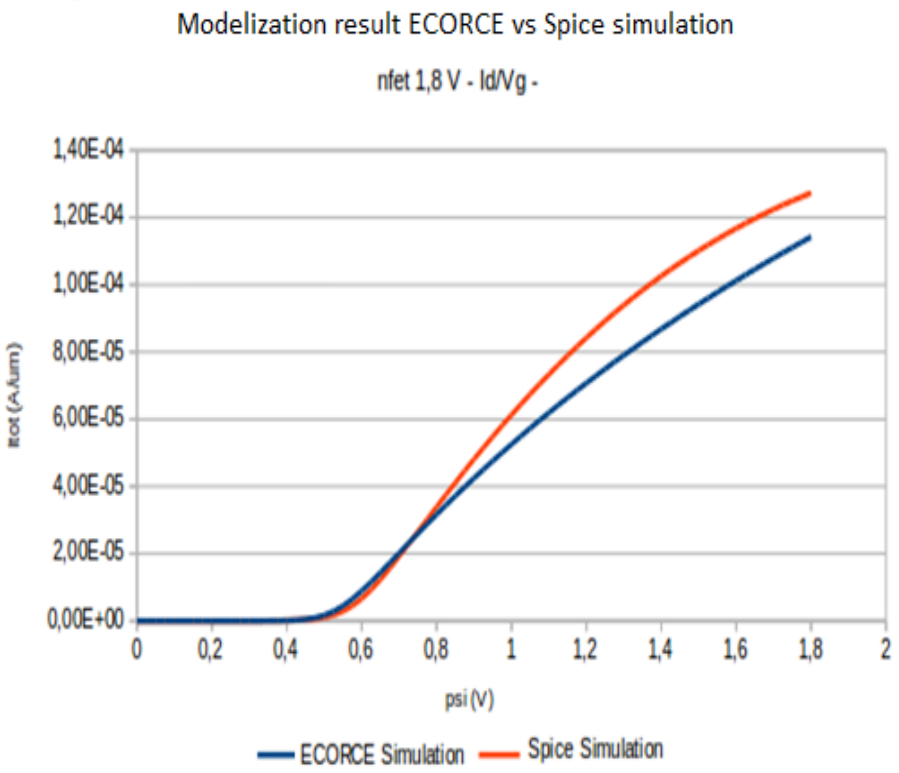


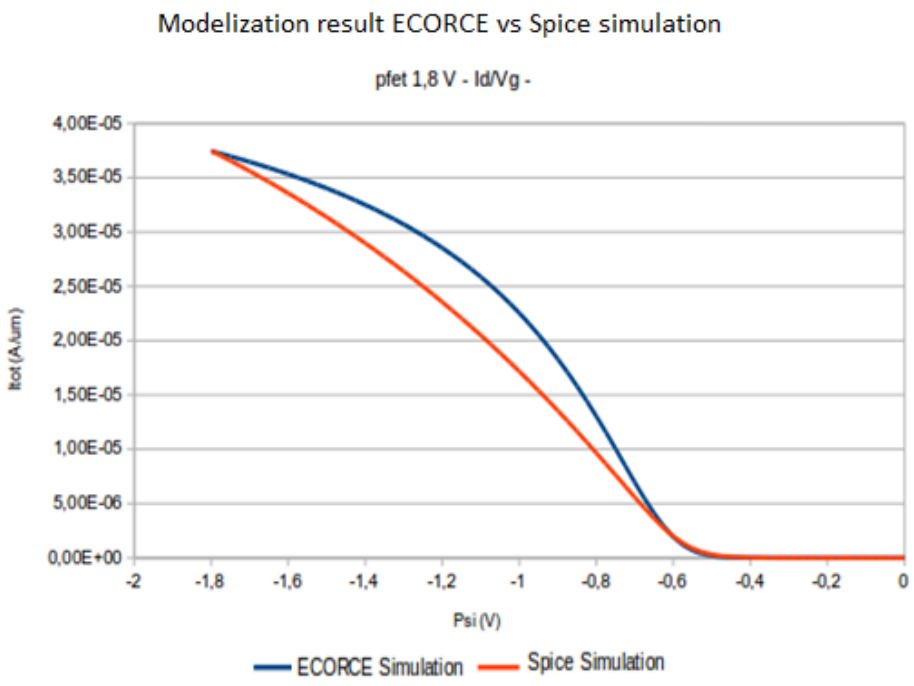
MOS transistor modeled with ECORCE

realese 3753 ECORCE

Study of the Atmel/MCP PDSOI150 nm technology

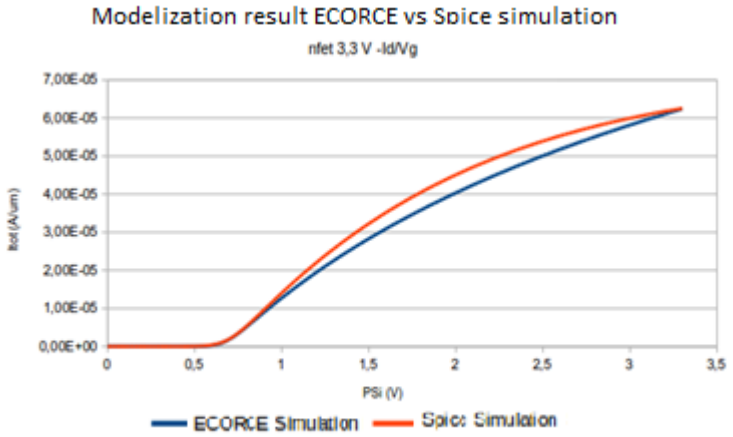
Preliminary results before integration of MOS technology doping profiles
1,8V

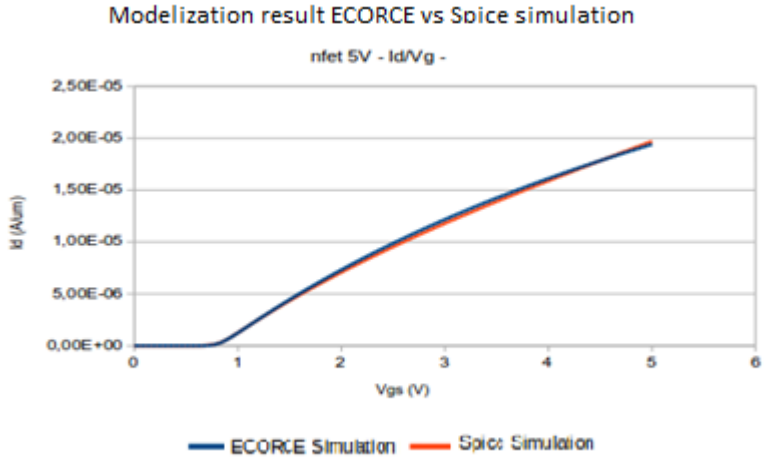


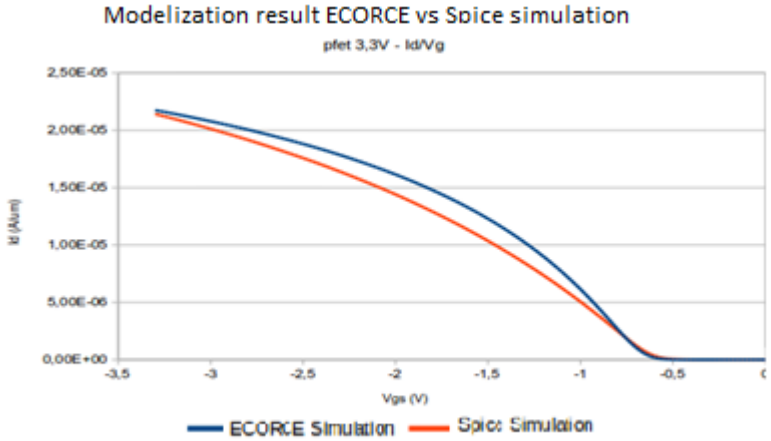


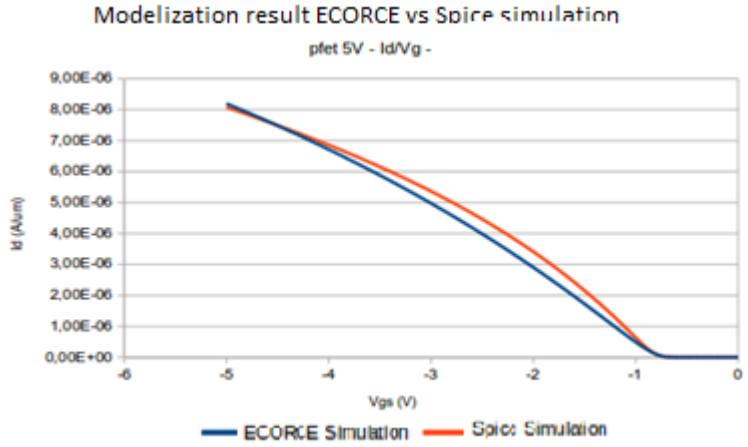
Study of the Atmel/MCP PDSOI150 nm technology

Preliminary results before integration of 3.3V and 5V MOS technology doping profiles





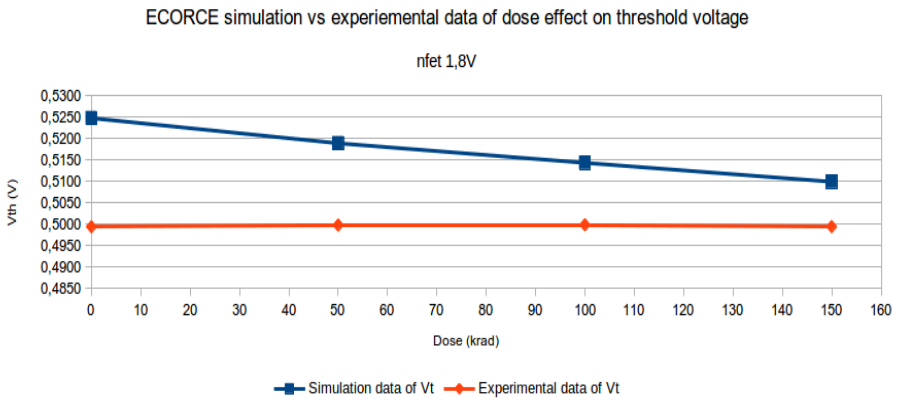


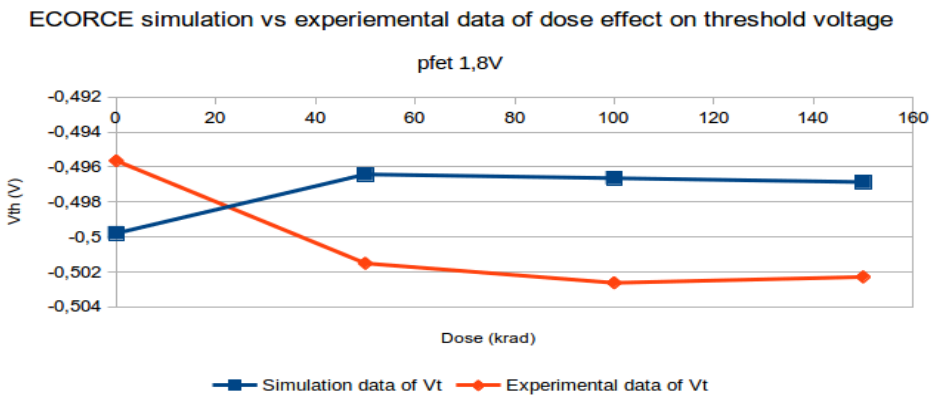


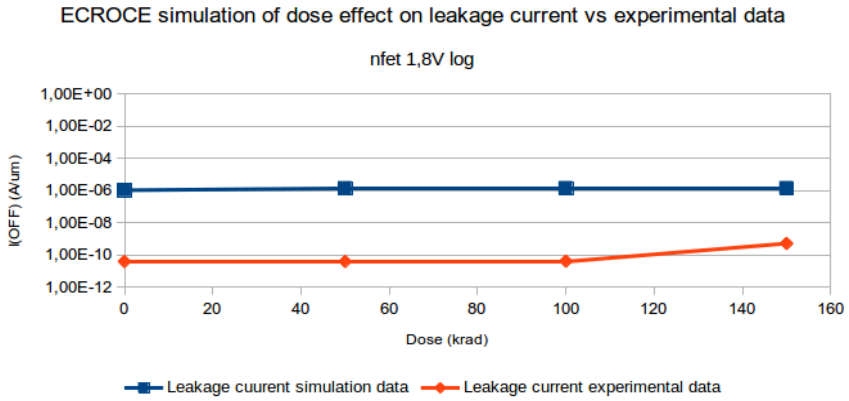
ECORCE

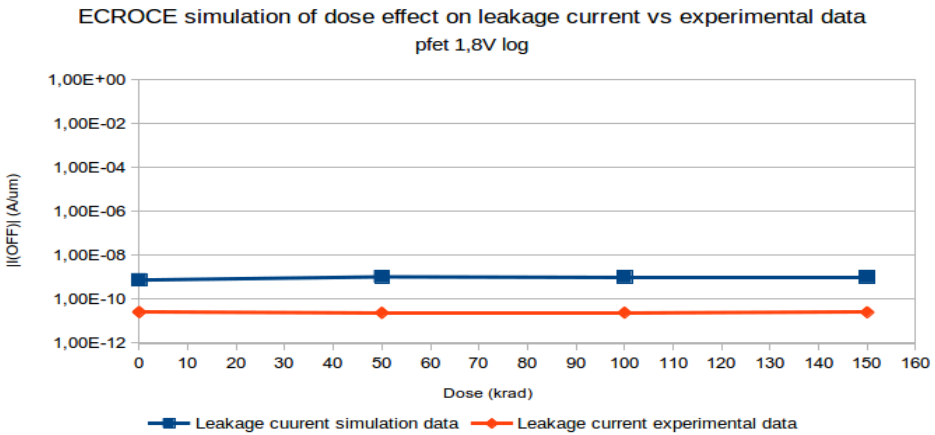
Study of the Atmel/MCP PDSOI150 nm technology

Preliminary results of the V_{th} et I_{off} dose simulation on the 1.8 V transistors
Before integration of doping profiles and optimized distribution of traps





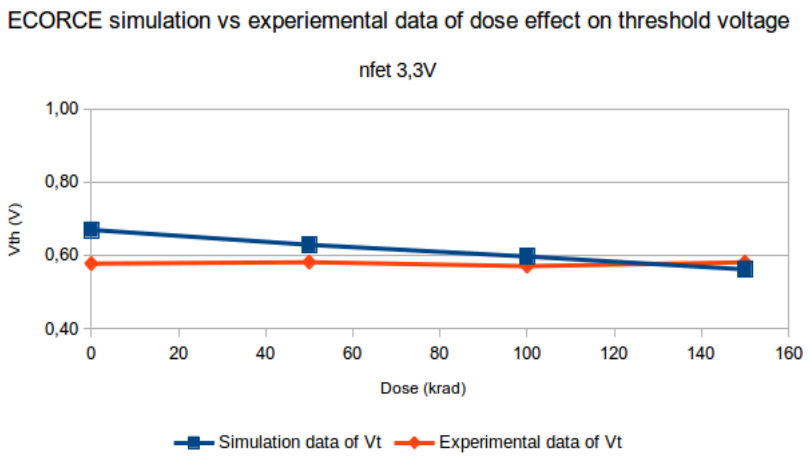


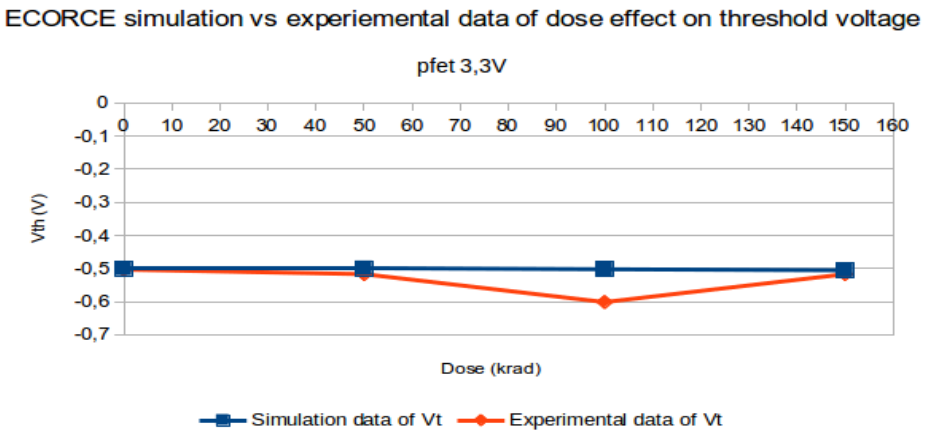


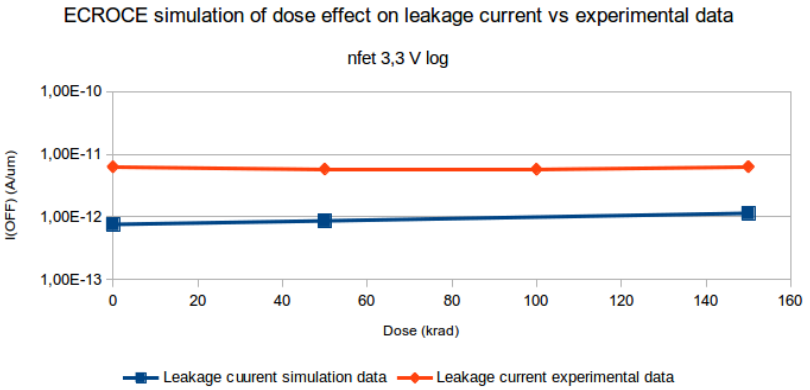
ECORCE

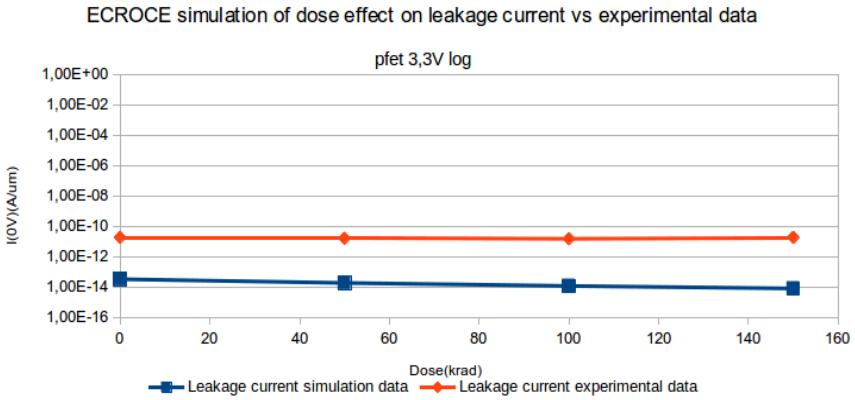
Study of the Atmel/MCP PDSOI150 nm technology

Preliminary results of the V_{th} et I_{off} dose simulation on the 3.3 V transistors
Before integration of doping profiles and optimized distribution of traps





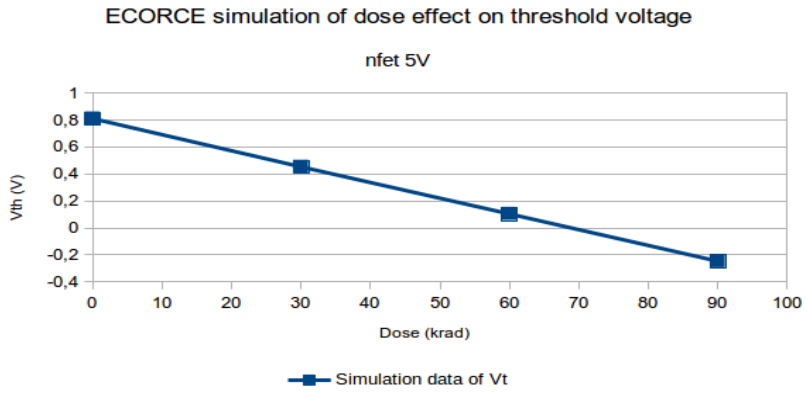


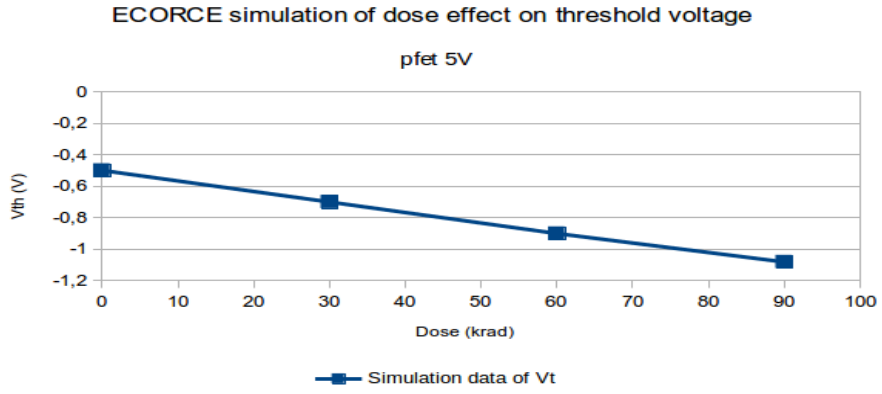


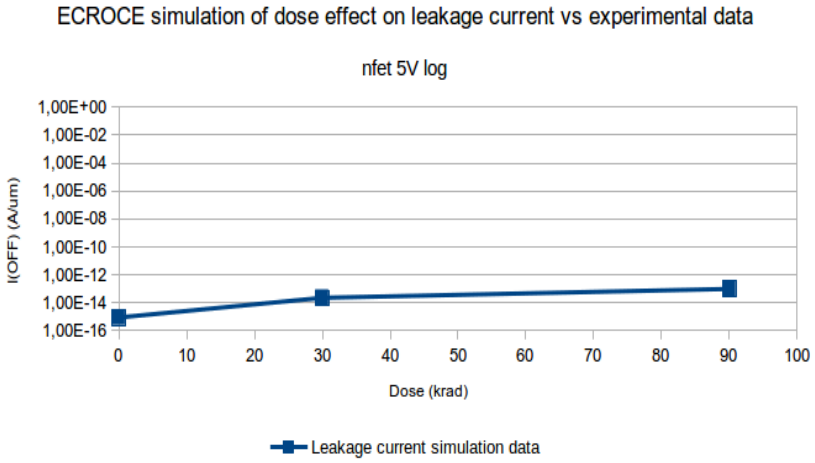
ECORCE

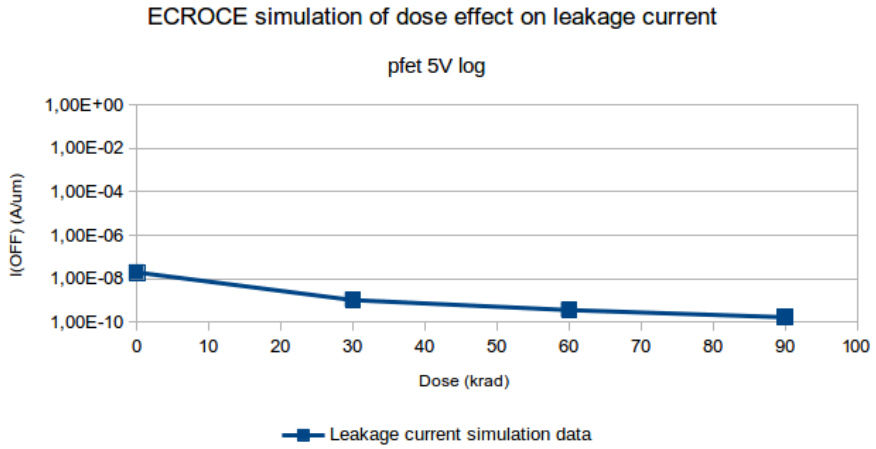
Study of the Atmel/MCP PDSOI150 nm technology

Preliminary results of the V_{th} et I_{off} dose simulation on the 5 V transistors
Before integration of doping profiles and optimized distribution of traps









Study of the Atmel/MCP PDSOI150 nm technology

- Simulation of the electrical behavior of transistors
  - Good coherence of Spice and ECORCE simulations
    - Percentage of error below a factor of 2 for the least well modeled cases
  - Validation of behaviors for integration of doping profiles for better optimization
- Simulation of the dose effect on components
  - The trends of the first dose modeling are in agreement with experiment
    - Distribution of traps to optimize

Conclusion : where am I ?

- Atmel/MCP 150nm PDSOI technology
  - Integration of realistic doping profile in ECORCE in progress
    - New electrical simulation
    - New TID simulation
    - Validation of ECORCE Tool
- FDSOI22 of Global Foundry nm technology
  - State of the art in progress
  - During this month
    - Starting the first model with ECORCE of FDSOI22 nm from GF
    - Implementation of the TID test plan

Thank you for your attention !

Backup slide

Bulk vs FDSOI

- There is a Ultra thinh Buried Oxide((UBOX) in a FDSOI
- To prevent against leakage current
- To prevent against several short channel effect [1]
- Imunize to the latch-up [2]
- Better efficiency in low voltage [3]

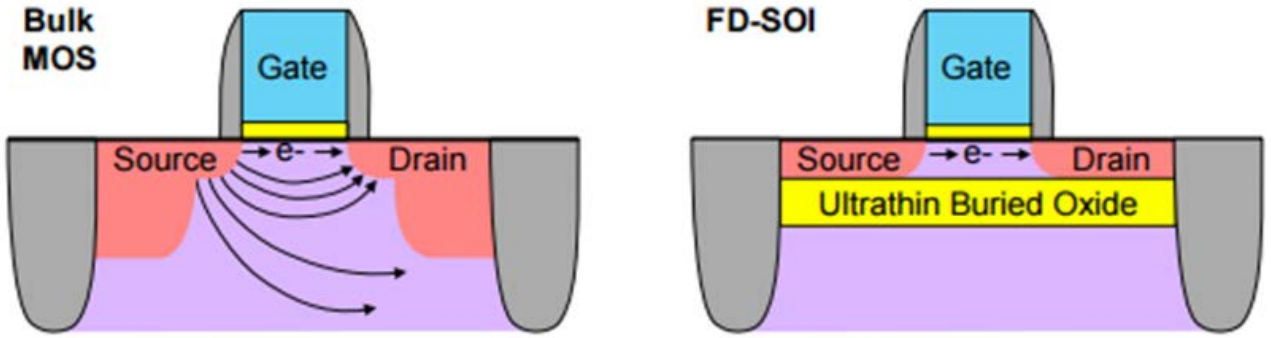


Figure 1. Traditional MOS versus FD-SOI.

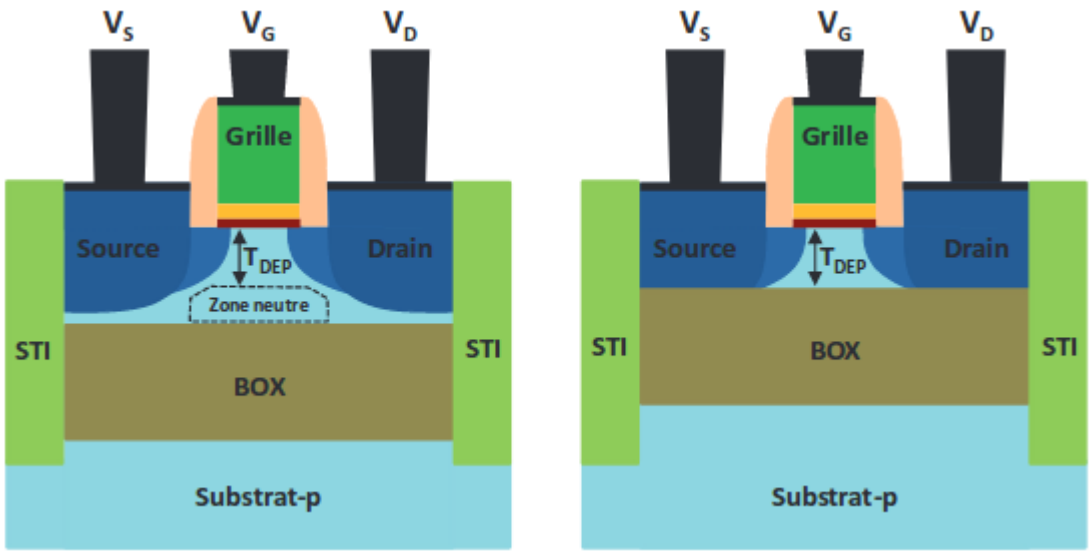
(1) X. Federspiel, D. Angot, M. Rafik, F. Cacho, A. Bajolet, N. Planes, D. Roy, M. Haond, and F. Arnaud. 28nm node bulk vs FDSOI reliability comparison. In IEEE International Reliability Physics Symposium Proceedings, pages 4–7, 2012.

(2) Jérome Mazurier. Etude de la variabilité en technologie FDSOI : du transistor aux cellules mémoires SRAM. 2012.

(3) Rida Kheirallah and Nadine Azemard. Energy Study for 28nm FDSOI Technology. Pages,23–26, 2015.

PDSOI vs FDSOI

- The size of the active area is the most important difference
- The size of the Box, usually thiner in a FDSOI
- The PDSOI technology allows devices with high voltage



PDSOI (left) vs FDSOI (right)